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Organic embedded architecture for sustainable FPGA soft-core processors
(2015) *Proceedings - Annual Reliability and Maintainability Symposium*, 2015-May, art. no. 7105065, .

Abstract
Mission-critical systems require increasing capability for fault handling and self-adaptation as their system complexities and inter-dependencies increase. Organic Computing (OC) architectures utilize biologically-inspired self-x properties which include self-configuration, self-reorganization, and self-healing which comprise the focus of this paper. To provide OC architectures with sufficient capability for exhibiting self-adaptive behavior, reconfigurable logic devices offer a suitable hardware platform. SRAM-based Field Programmable Gate Array (FPGA) logic devices can realize self-adaptation within their reconfigurable logic fabric using Evolvable Hardware techniques based on crossover, mutation, and iterative selection with intrinsic fitness assessment of the underlying hardware resources. In this paper, a dual-layer Organic Computing architecture called the Organic Embedded System (OES) is prototyped on a Xilinx FPGA reconfigurable fabric and assessed for maintainability metrics of completeness of repair, repair time, and degraded throughput during the repair phase. The approach used extends a widely known generic OC platform consisting of two layers: the Functional Layer and the Autonomic Layer. The Autonomic layer contains Autonomic Elements (AEs) that are responsible for correct operation of the corresponding Functional Elements (FEs) present on the Functional Layer. Innovations include autonomously degraded online throughput during regeneration, spare configuration aging and outlier driven repair assessment, and a uniform design for AEs despite the fact that they monitor different types of FEs. Using the OES approach; a malfunctioning or faulty AE among the population can be distinguished by its discrepant performance. The OES approach is implemented using high-level Hardware Description Language (HDL) which directs a Supervisor Element (SE) to function as a fault management unit through the collection of AE information. Experimental results show that the OES Autonomic Layer demonstrates 100% faulty component isolation for both FEs and AEs with randomly injected single faults. Using logic circuits from the MCNC-91 benchmark test set, throughput during repair phases averaged 75.05%, 82.21%, and 65.21% for the z4ml (2-bit adder), cm85a (high fan-in combinational logic), and cm138a (balanced I/O combinational logic) circuits respectively under stated conditions. © 2015 IEEE.

2-s2.0-84945382553
Document Type: Conference Paper
Publication Stage: Final
Source: Scopus